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PATENT NUMBER and  
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10077967	FILING DATE 02/20/2002	CLASS 438 257	SUBCLASS 107	GAU 2822	EXAMINER TRINH
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\*\*APPLICANTS: Kim Sarah; List R.; Kellar Scot;

\*\*CONTINUING DATA VERIFIED: MT none)

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\*\* FOREIGN APPLICATIONS VERIFIED: MT none

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no	ATTORNEY DOCKET NO
35 USC 119 conditions met	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no	219.40232X00
Verified and Acknowledged Examiners's initials MT		
TITLE : Process of vertically stacking multiple wafers supporting different active integrated circuit (IC) devices		

U.S. DEPT. OF COMM./PAT. & TM.-PTO-435L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G
Assistant Examiner		DRAWING	
		Shoote Drwg.	Figs. Drwg. Print Fig.
ISSUE FEE		Applicati n Examiner	
Amount Due	Date Paid		
Primary Examiner			
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	
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